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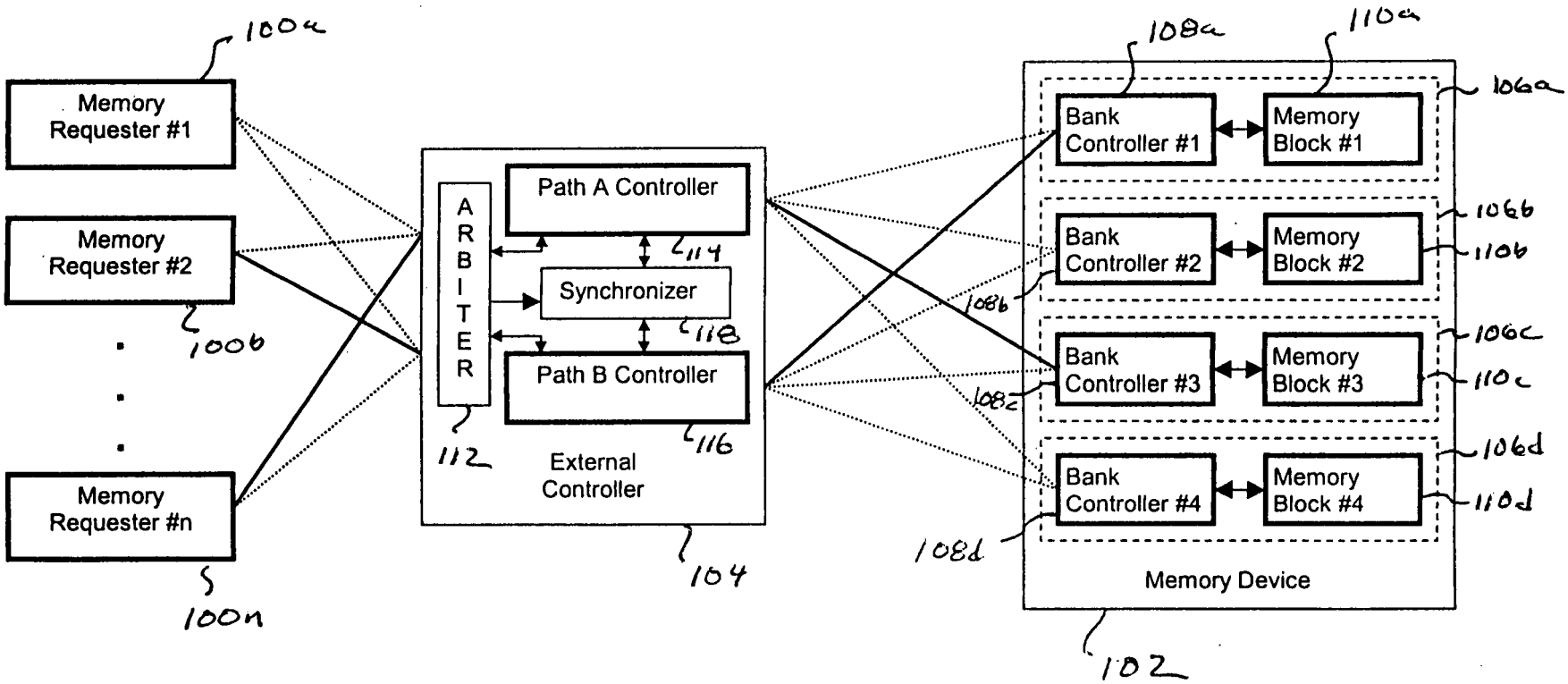
Memory Requester #1
Memory Requester #2
Memory Requester #n
100a
100b
100n
ARBITER
Path A Controller
Synchronizer
Path B Controller
114
118
116
112
External Controller
104
108a
110a
106a
Bank Controller #1
Memory Block #1
106b
Bank Controller #2
Memory Block #2
110b
108b
106c
Bank Controller #3
Memory Block #3
110c
108c
106d
Bank Controller #4
Memory Block #4
110d
108d
Memory Device
102

FIG. 1

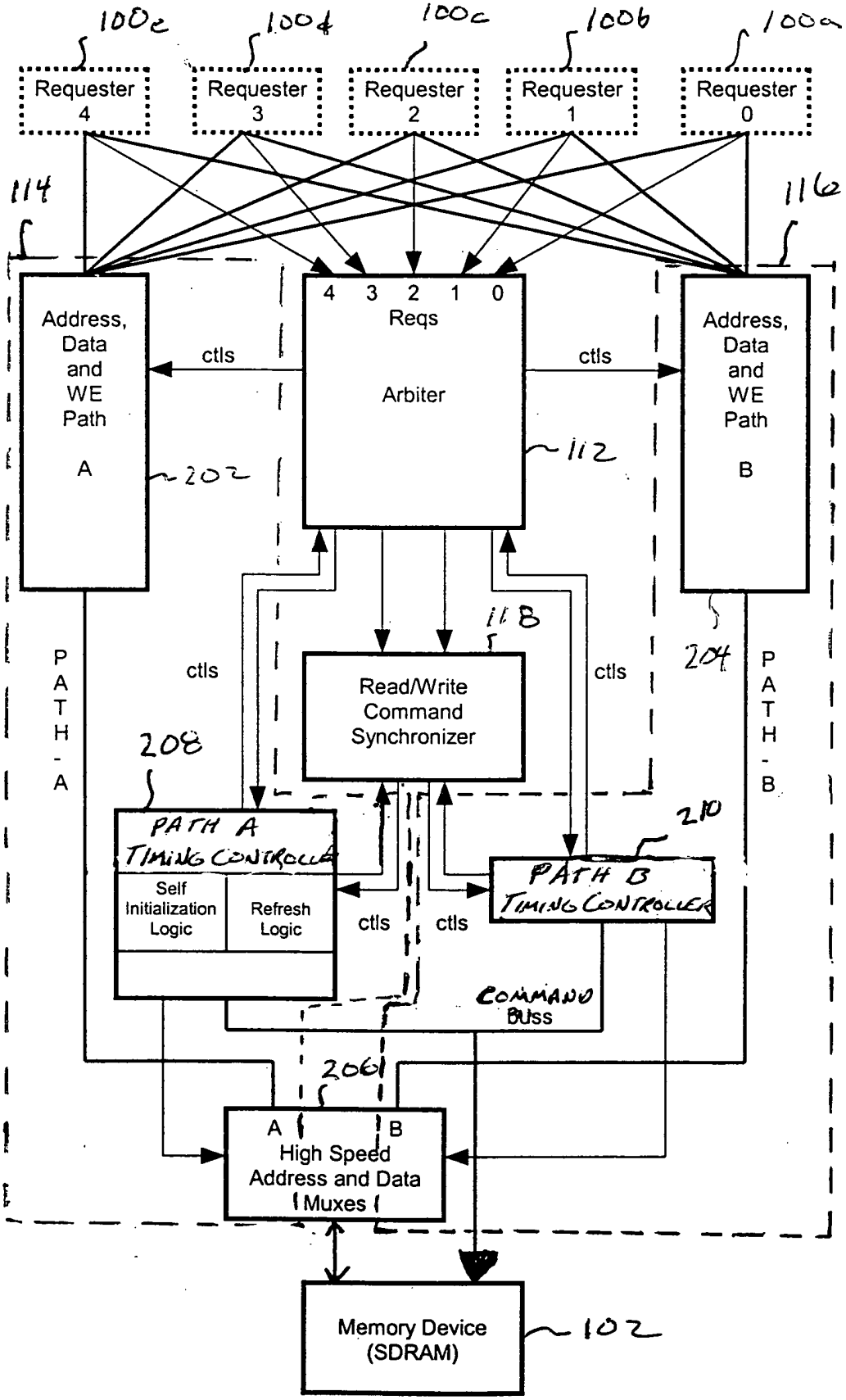
100e
100d
100c
100b
100a
Requester 4
Requester 3
Requester 2
Requester 1
Requester 0
114
116
Address, Data and WE Path A
202
4 3 2 1 0
Reqs
Arbiter
112
ctls
ctls
Address, Data and WE Path B
118
204
PATH-A
ctls
Read/Write Command Synchronizer
ctls
PATH-B
208
PATH A TIMING CONTROLLER
Self Initialization Logic
Refresh Logic
210
PATH B TIMING CONTROLLER
ctls
ctls
COMMAND BUSS
206
A
B
High Speed Address and Data Muxes
Memory Device (SDRAM)
102

FIG. 2

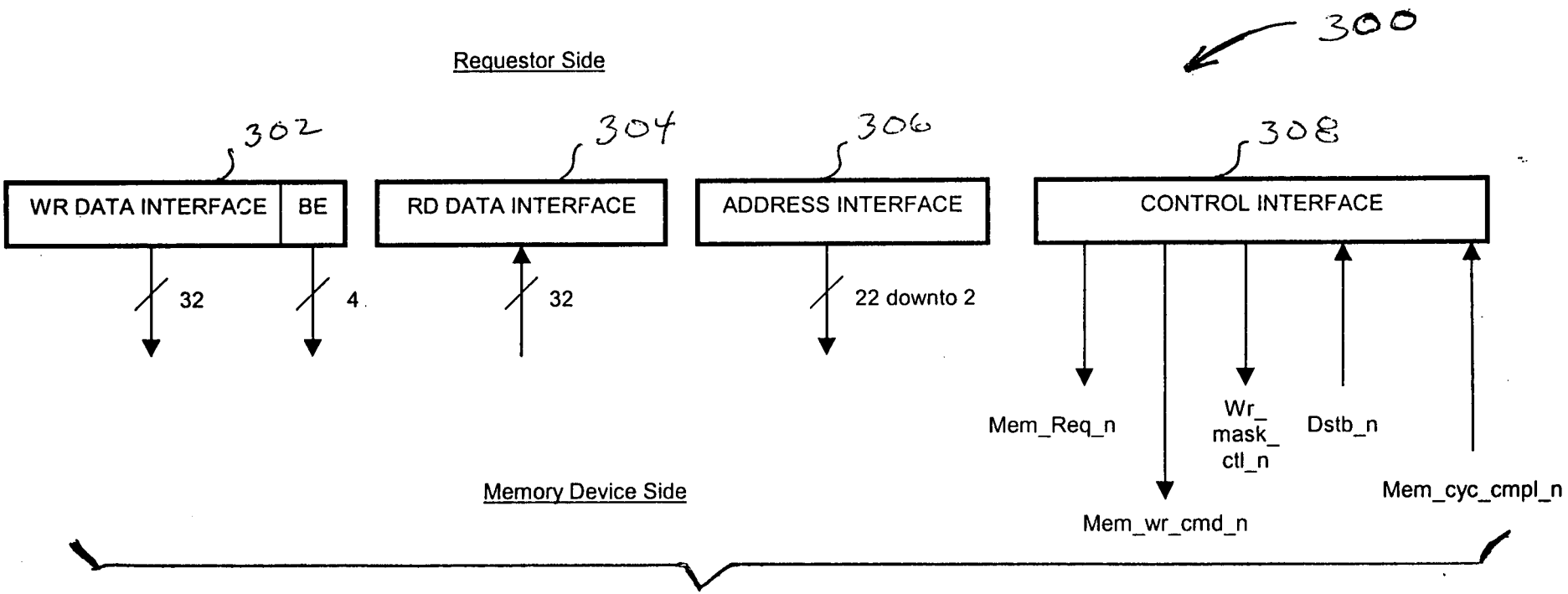
300
Requestor Side
302
304
306
308
WR DATA INTERFACE
BE
RD DATA INTERFACE
ADDRESS INTERFACE
CONTROL INTERFACE
32
4
32
22 downto 2
Mem_Req_n
Wr_ mask_ ctl_n
Dstb_n
Mem_cyc_cmpl_n
Memory Device Side
Mem_wr_cmd_n

FIG. 3

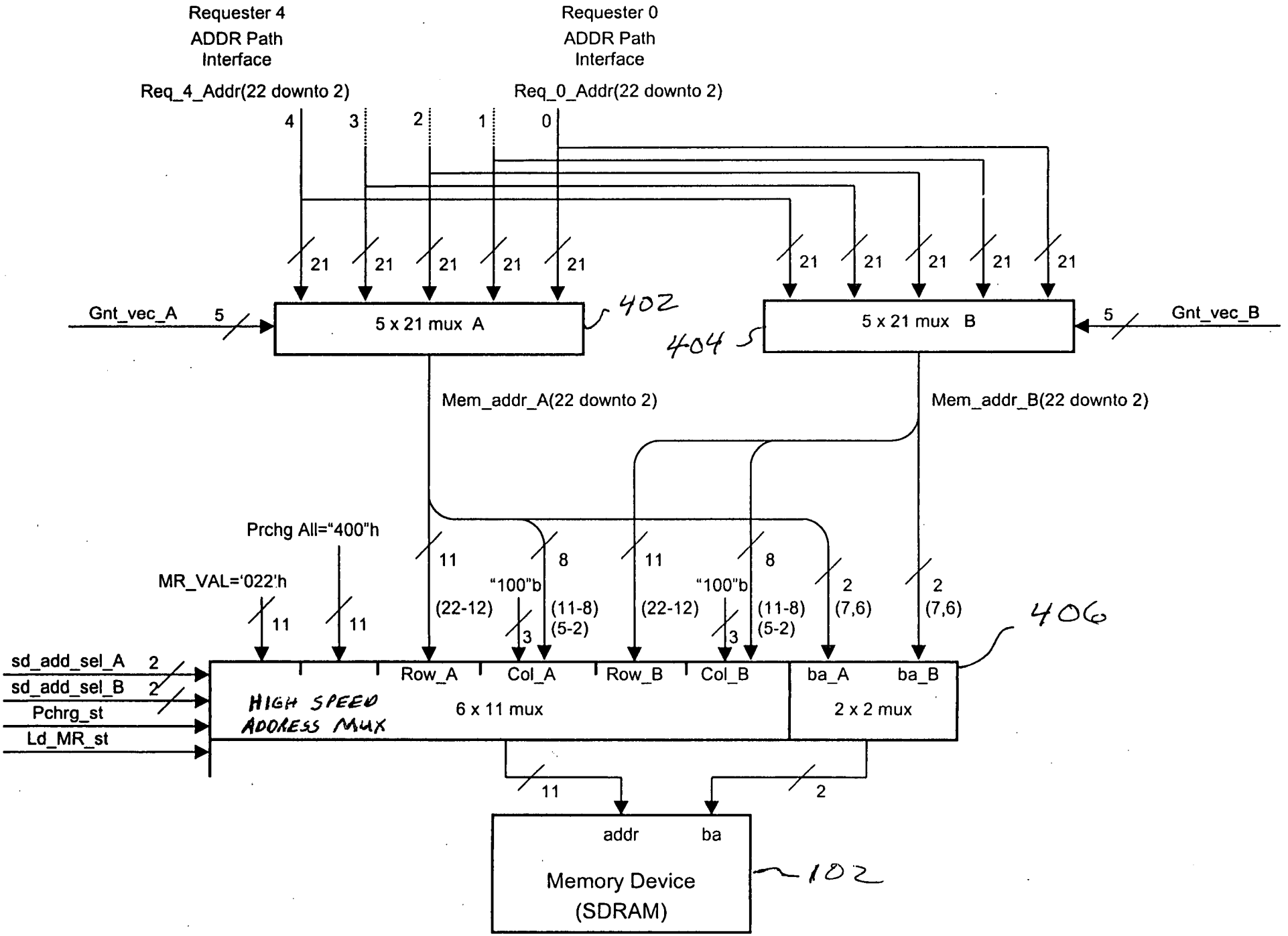
Requester 4
ADDR Path
Interface
Req_4_Addr(22 downto 2)
Requester 0
ADDR Path
Interface
Req_0_Addr(22 downto 2)
4
3
2
1
0
21
Gnt_vec_A
5
5 x 21 mux A
402
404
5 x 21 mux B
Gnt_vec_B
Mem_addr_A(22 downto 2)
Mem_addr_B(22 downto 2)
Prchg All="400"h
MR_VAL='022'h
11
8
"100"b
3
(22-12)
(11-8)
(5-2)
2
(7,6)
406
sd_add_sel_A
sd_add_sel_B
Pchrg_st
Ld_MR_st
Row_A
Col_A
Row_B
Col_B
ba_A
ba_B
HIGH SPEED
ADDRESS MUX
6 x 11 mux
2 x 2 mux
addr
ba
Memory Device
(SDRAM)
102

FIG. 4

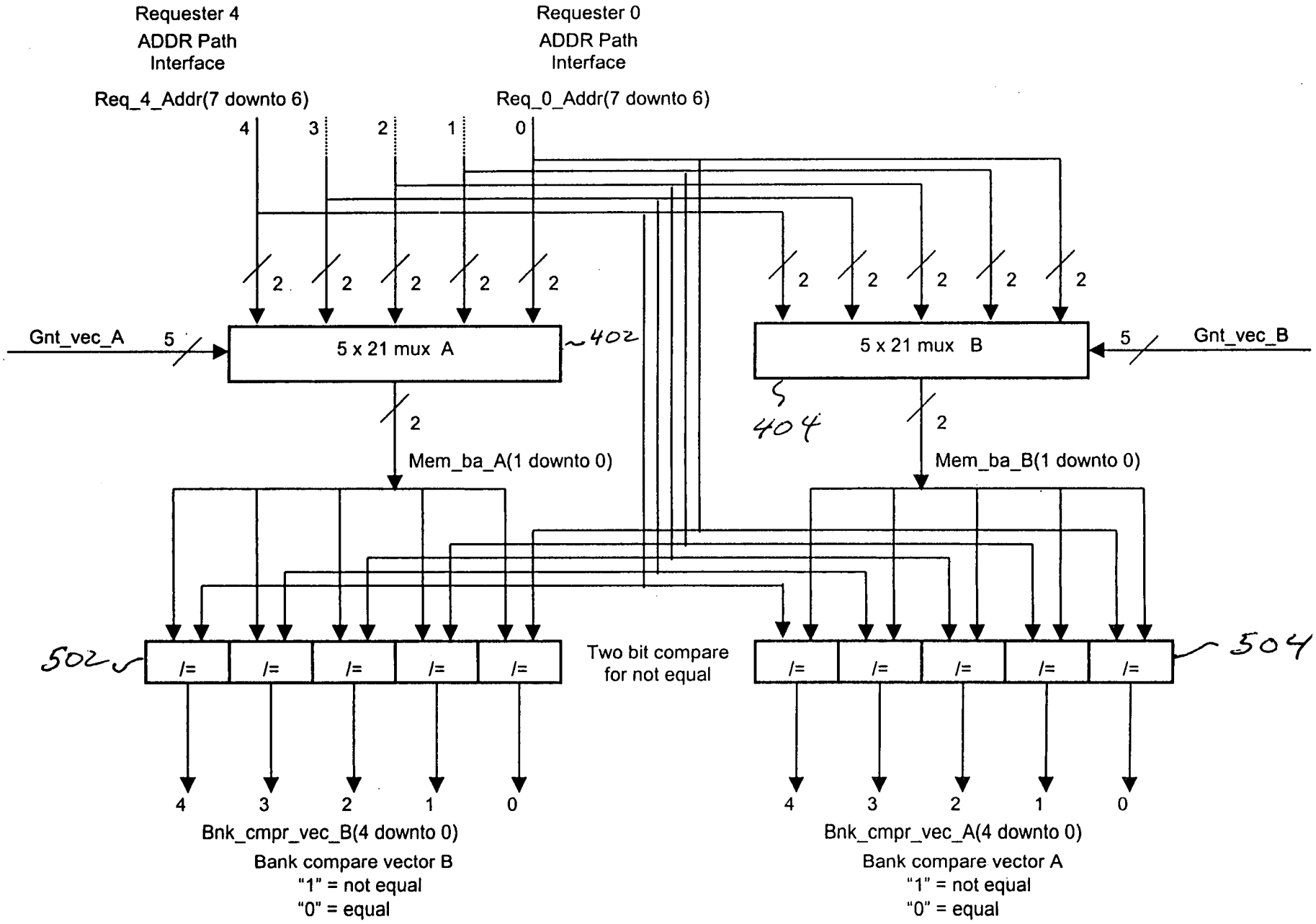
Requester 4
ADDR Path
Interface
Requester 0
ADDR Path
Interface
Req_4_Addr(7 downto 6)
Req_0_Addr(7 downto 6)
4
3
2
1
0
2
Gnt_vec_A
5
5 x 21 mux A
402
5 x 21 mux B
Gnt_vec_B
404
Mem_ba_A(1 downto 0)
Mem_ba_B(1 downto 0)
502
/=
Two bit compare
for not equal
504
Bnk_cmpr_vec_B(4 downto 0)
Bank compare vector B
"1" = not equal
"0" = equal
Bnk_cmpr_vec_A(4 downto 0)
Bank compare vector A
"1" = not equal
"0" = equal

FIG. 5

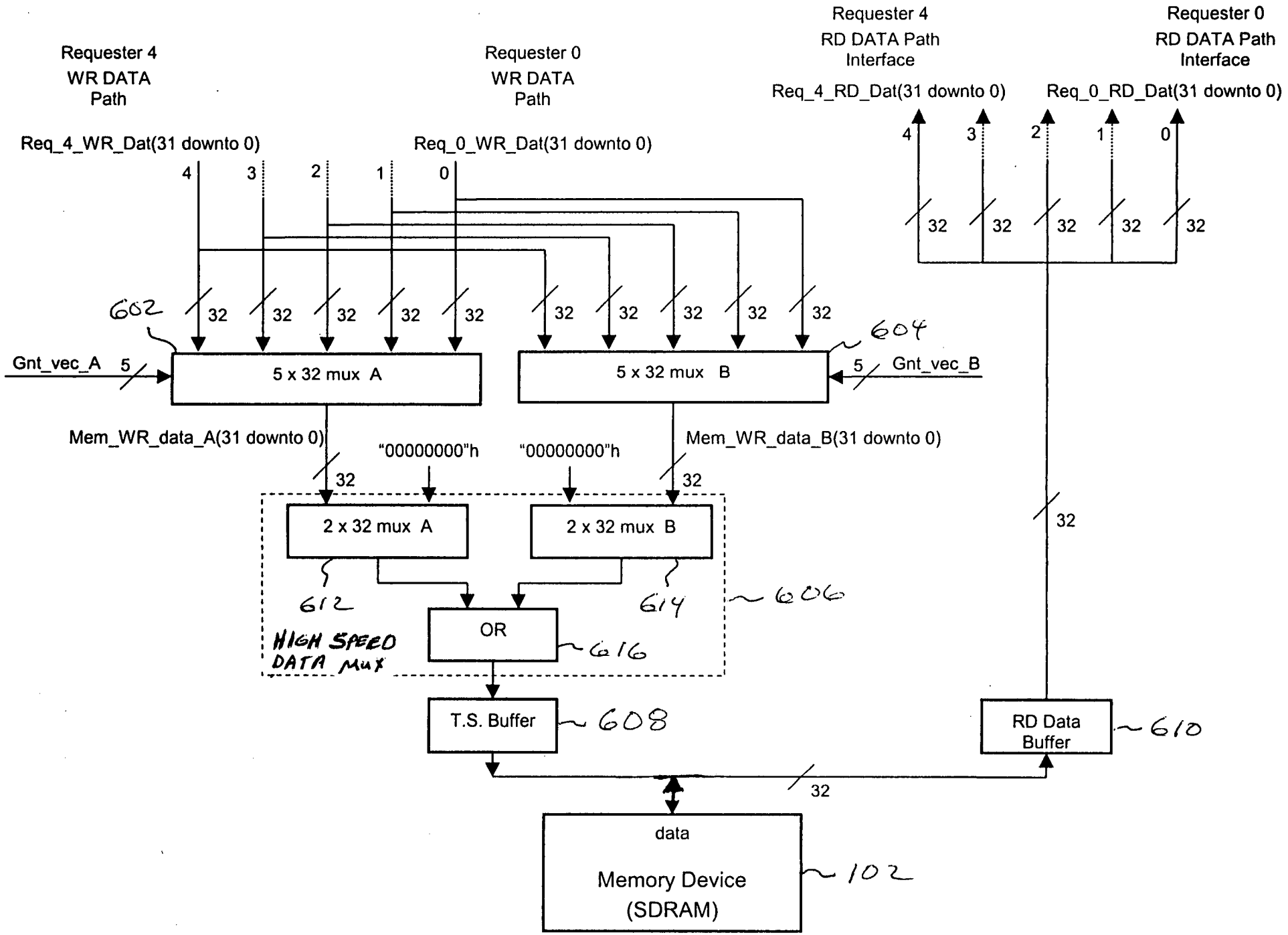
Requester 4
WR DATA
Path
Requester 0
WR DATA
Path
Requester 4
RD DATA Path
Interface
Requester 0
RD DATA Path
Interface
Req_4_WR_Dat(31 downto 0)
Req_0_WR_Dat(31 downto 0)
Req_4_RD_Dat(31 downto 0)
Req_0_RD_Dat(31 downto 0)
4
3
2
1
0
32
602
604
Gnt_vec_A
5
5 x 32 mux A
5 x 32 mux B
5
Gnt_vec_B
Mem_WR_data_A(31 downto 0)
"00000000"h
"00000000"h
Mem_WR_data_B(31 downto 0)
2 x 32 mux A
2 x 32 mux B
612
614
606
HIGH SPEED
DATA MUX
OR
616
T.S. Buffer
608
RD Data
Buffer
610
data
Memory Device
(SDRAM)
102

FIG. 6

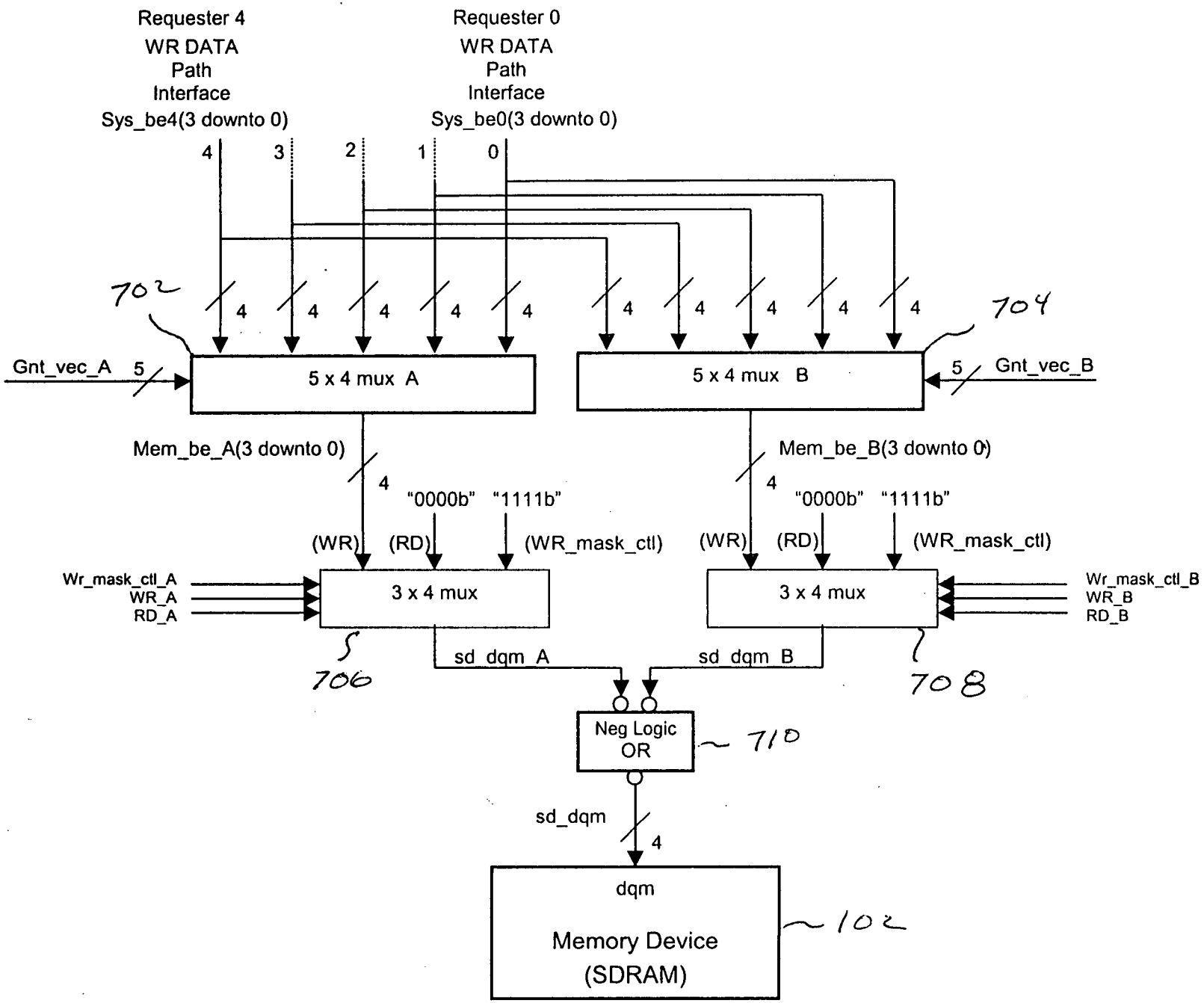
Requester 4
WR DATA
Path
Interface
Sys_be4(3 downto 0)
Requester 0
WR DATA
Path
Interface
Sys_be0(3 downto 0)
4
3
2
1
0
702
704
Gnt_vec_A
5
5 x 4 mux A
5 x 4 mux B
5
Gnt_vec_B
Mem_be_A(3 downto 0)
Mem_be_B(3 downto 0)
"0000b"
"1111b"
(WR)
(RD)
(WR_mask_ctl)
Wr_mask_ctl_A
WR_A
RD_A
3 x 4 mux
3 x 4 mux
Wr_mask_ctl_B
WR_B
RD_B
706
708
sd_dqm_A
sd_dqm_B
Neg Logic
OR
710
sd_dqm
dqm
Memory Device
(SDRAM)
102

FIG. 7

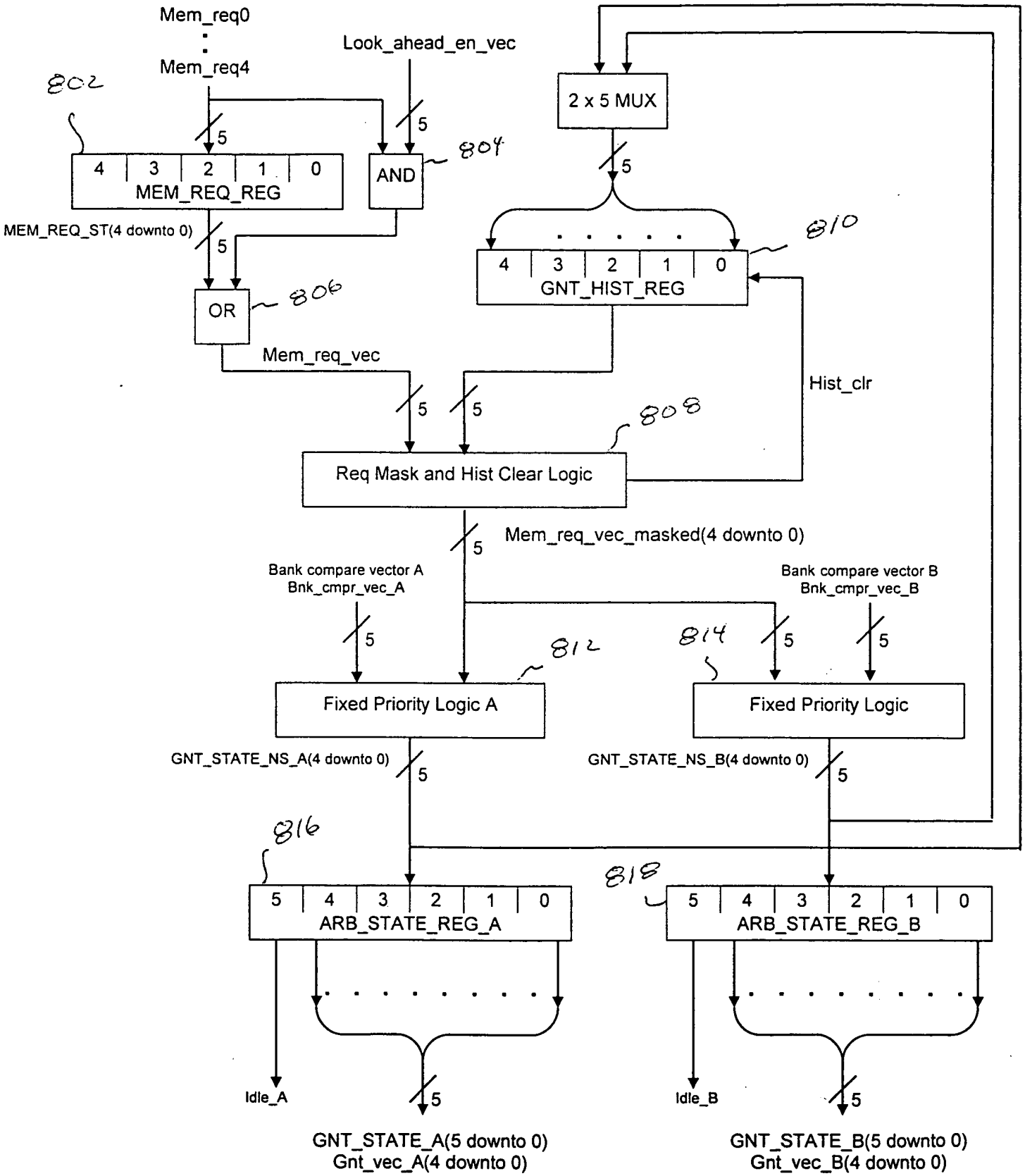
Mem_req0
Mem_req4
Look_ahead_en_vec
802
804
2 x 5 MUX
MEM_REQ_REG
AND
MEM_REQ_ST(4 downto 0)
810
GNT_HIST_REG
OR
806
Mem_req_vec
Hist_clr
808
Req Mask and Hist Clear Logic
Mem_req_vec_masked(4 downto 0)
Bank compare vector A
Bnk_cmpr_vec_A
Bank compare vector B
Bnk_cmpr_vec_B
812
814
Fixed Priority Logic A
Fixed Priority Logic
GNT_STATE_NS_A(4 downto 0)
GNT_STATE_NS_B(4 downto 0)
816
818
ARB_STATE_REG_A
ARB_STATE_REG_B
Idle_A
Idle_B
GNT_STATE_A(5 downto 0)
Gnt_vec_A(4 downto 0)
GNT_STATE_B(5 downto 0)
Gnt_vec_B(4 downto 0)

FIG 8

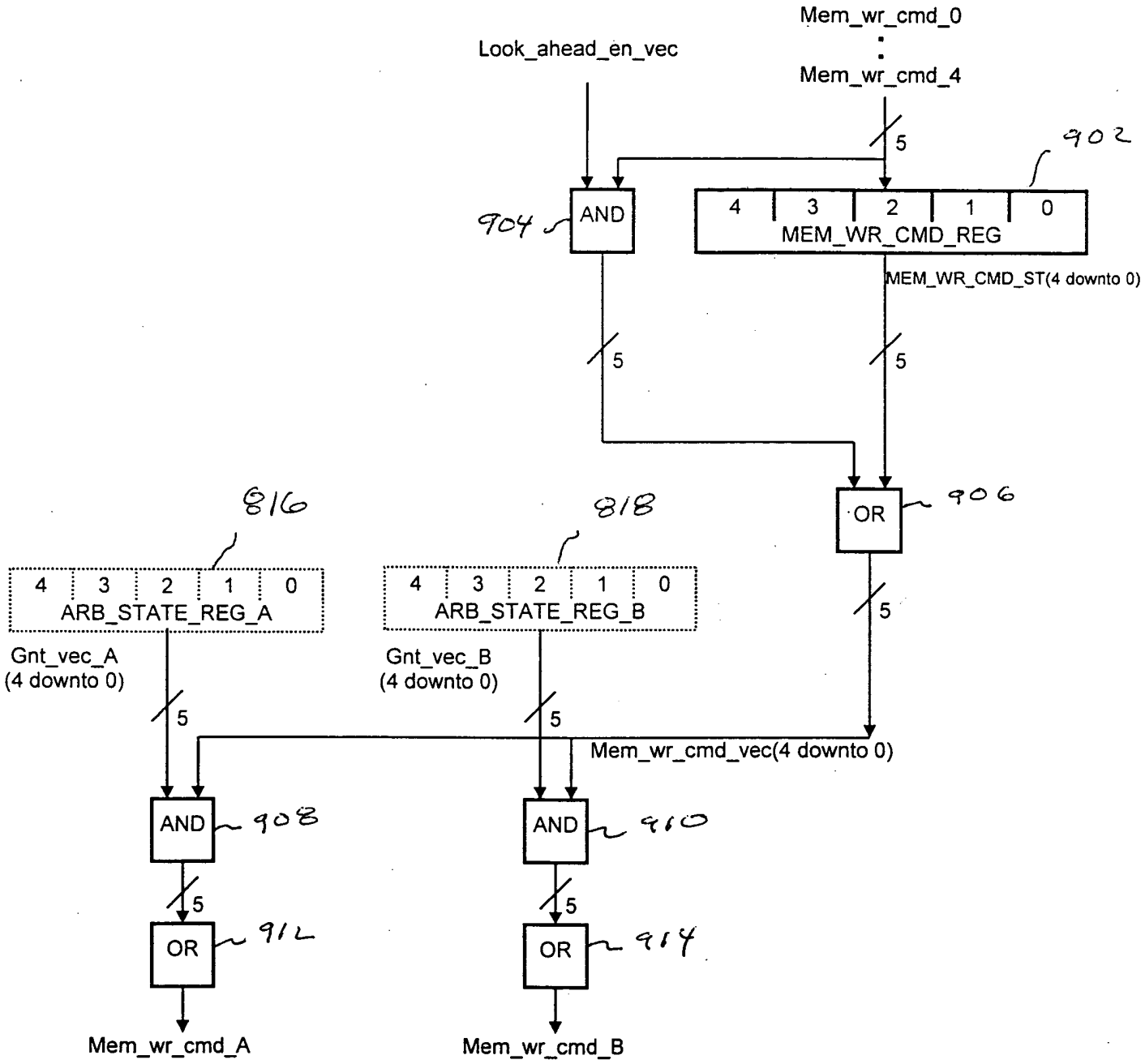
Mem_wr_cmd_0
Look_ahead_en_vec
Mem_wr_cmd_4
5
902
904
AND
4 3 2 1 0
MEM_WR_CMD_REG
MEM_WR_CMD_ST(4 downto 0)
5
5
OR
906
816
818
4 3 2 1 0
ARB_STATE_REG_A
4 3 2 1 0
ARB_STATE_REG_B
Gnt_vec_A
(4 downto 0)
Gnt_vec_B
(4 downto 0)
5
5
5
Mem_wr_cmd_vec(4 downto 0)
AND
908
AND
910
5
5
OR
912
OR
914
Mem_wr_cmd_A
Mem_wr_cmd_B

FIG 9

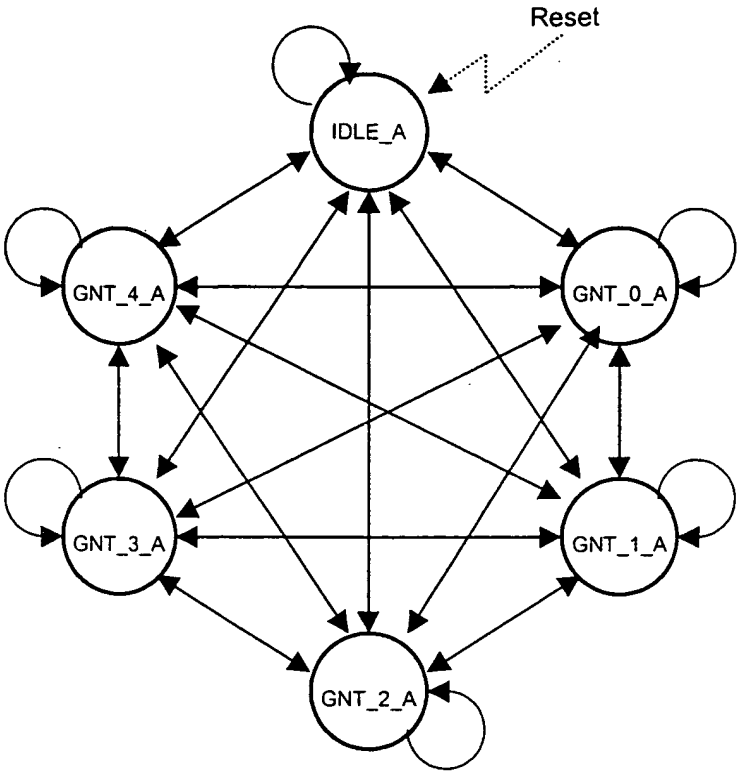

FIG. 10A

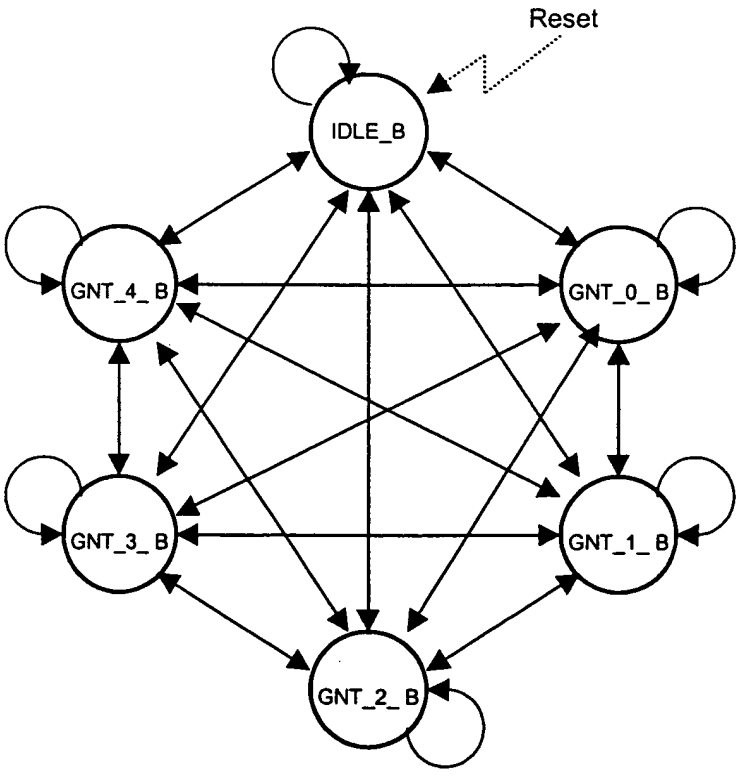

FIG. 10B

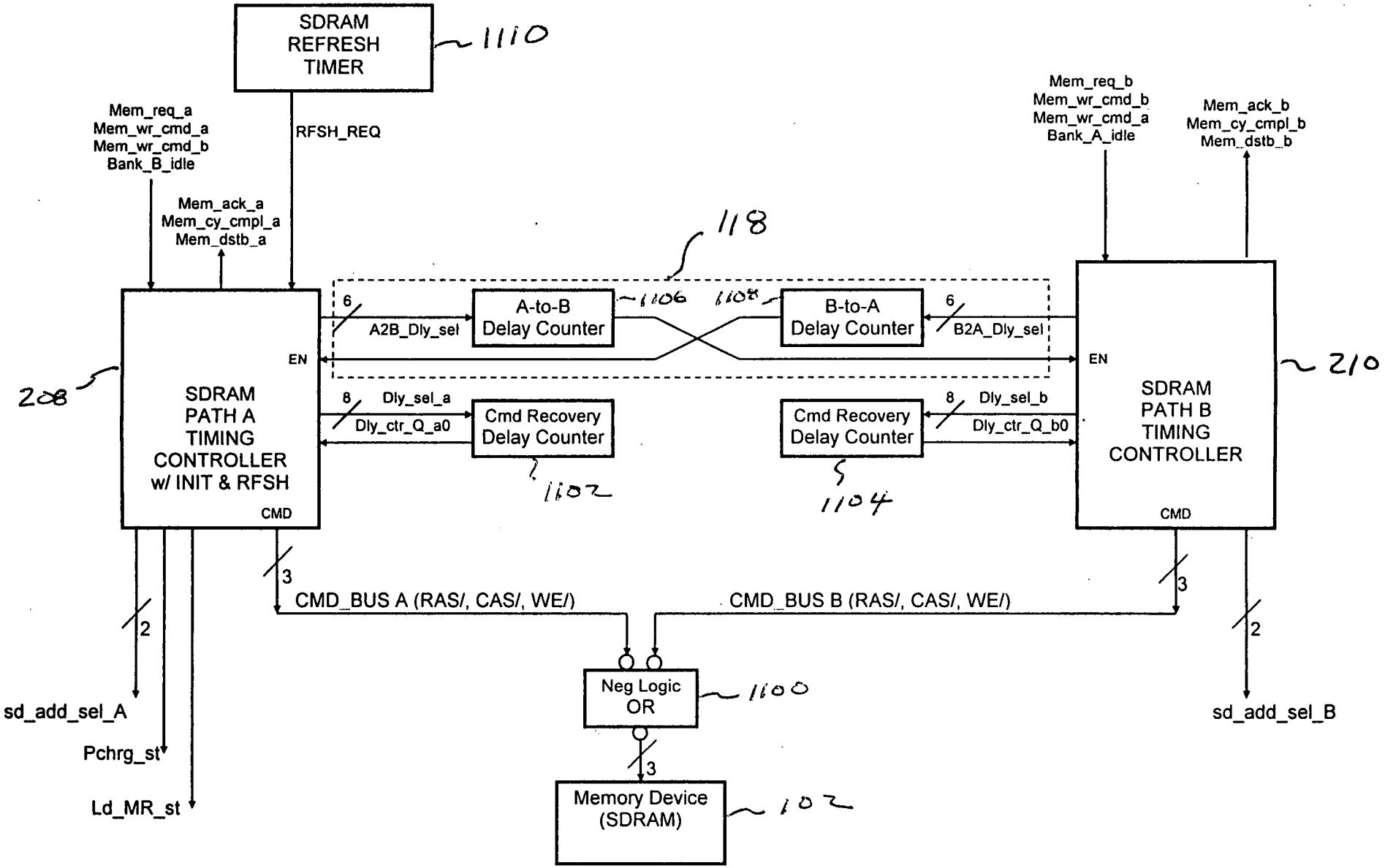
SDRAM REFRESH TIMER
1110
RFSH_REQ
Mem_req_a
Mem_wr_cmd_a
Mem_wr_cmd_b
Bank_B_idle
Mem_ack_a
Mem_cy_cmpl_a
Mem_dstb_a
118
6
A2B_Dly_sel
A-to-B Delay Counter
1106
1108
B-to-A Delay Counter
6
B2A_Dly_sel
EN
208
SDRAM PATH A TIMING CONTROLLER w/ INIT & RFSH
CMD
8
Dly_sel_a
Dly_ctr_Q_a0
Cmd Recovery Delay Counter
1102
Cmd Recovery Delay Counter
8
Dly_sel_b
Dly_ctr_Q_b0
1104
Mem_req_b
Mem_wr_cmd_b
Mem_wr_cmd_a
Bank_A_idle
Mem_ack_b
Mem_cy_cmpl_b
Mem_dstb_b
EN
SDRAM PATH B TIMING CONTROLLER
210
CMD
3
CMD_BUS A (RAS/, CAS/, WE/)
CMD_BUS B (RAS/, CAS/, WE/)
3
2
2
sd_add_sel_A
Pchrg_st
Ld_MR_st
sd_add_sel_B
Neg Logic OR
1100
3
Memory Device (SDRAM)
102

FIG. 11

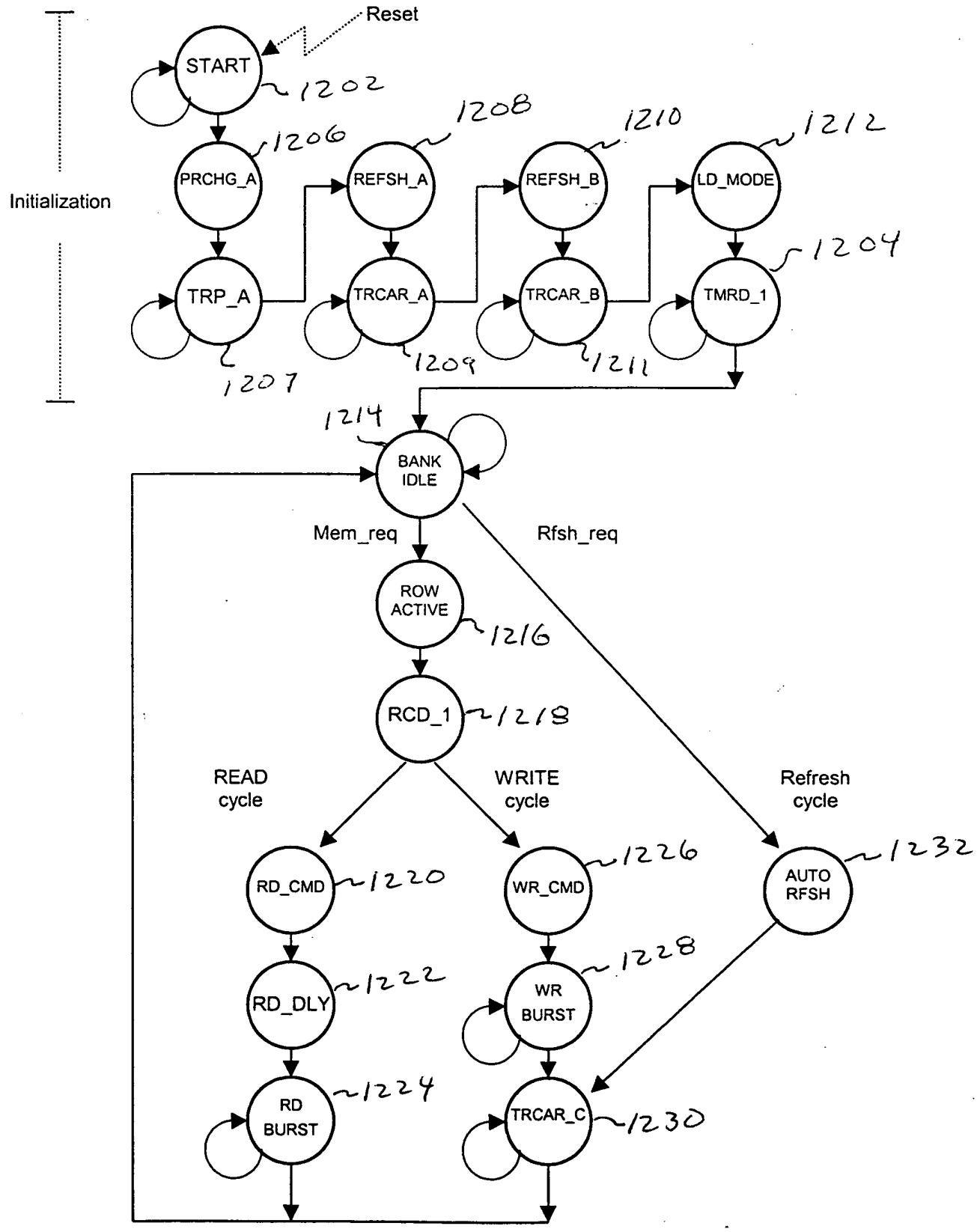
Reset
START
1202
Initialization
PRCHG_A
1206
REFSH_A
1208
REFSH_B
1210
LD_MODE
1212
TRP_A
1207
TRCAR_A
1209
TRCAR_B
1211
TMRD_1
1204
1214
BANK IDLE
Mem_req
Rfsh_req
ROW ACTIVE
1216
RCD_1
1218
READ cycle
WRITE cycle
Refresh cycle
RD_CMD
1220
WR_CMD
1226
AUTO RFSH
1232
RD_DLY
1222
WR BURST
1228
RD BURST
1224
TRCAR_C
1230

FIG. 12

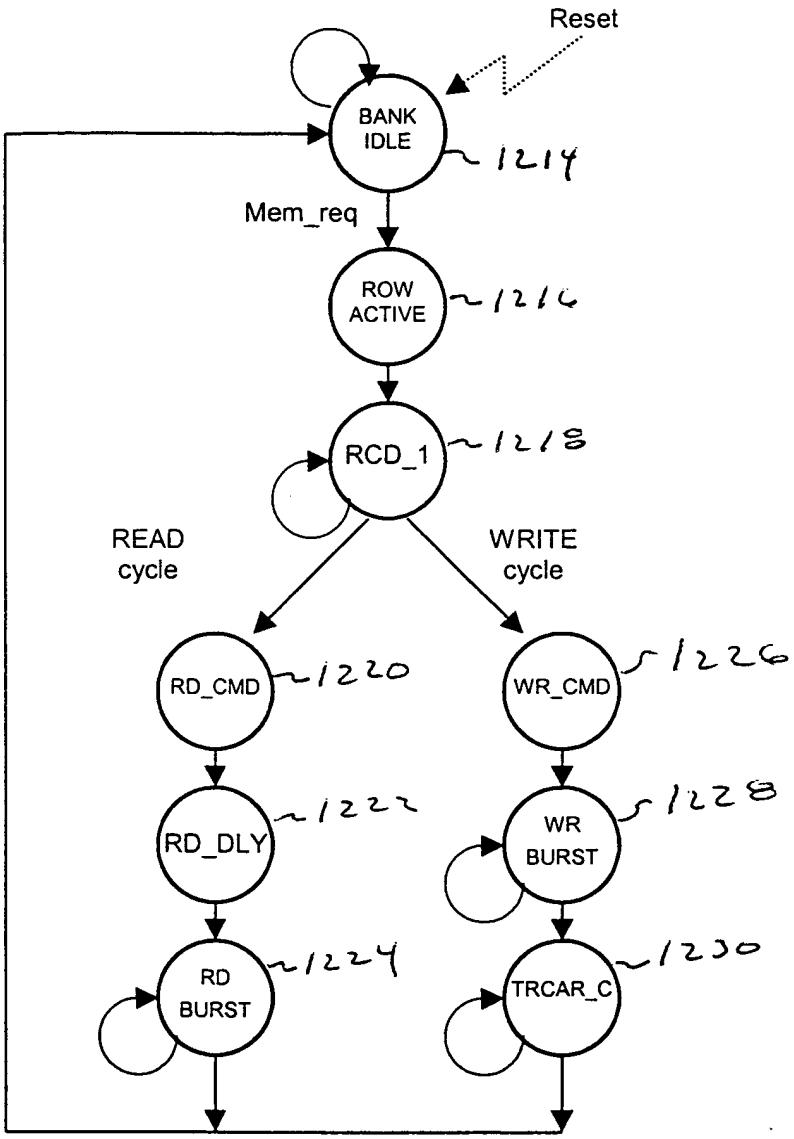
Reset
BANK IDLE
1214
Mem_req
ROW ACTIVE
1216
RCD_1
1218
READ cycle
WRITE cycle
RD_CMD
1220
WR_CMD
1226
RD_DLY
1222
WR BURST
1228
RD BURST
1224
TRCAR_C
1230

FIG. 13

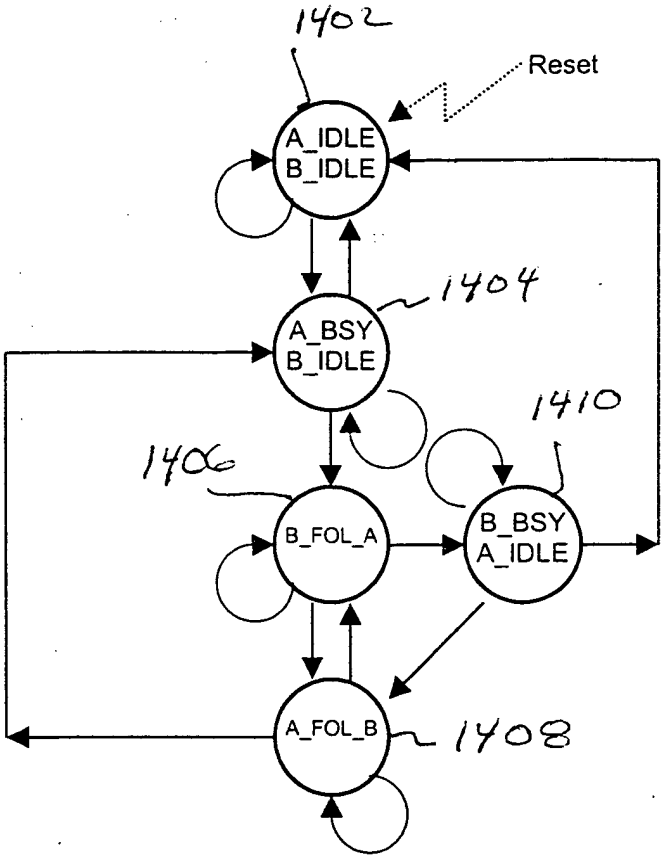
1402
Reset
A_IDLE
B_IDLE
1404
A_BSY
B_IDLE
1410
1406
B_FOL_A
B_BSY
A_IDLE
A_FOL_B
1408

FIG. 14

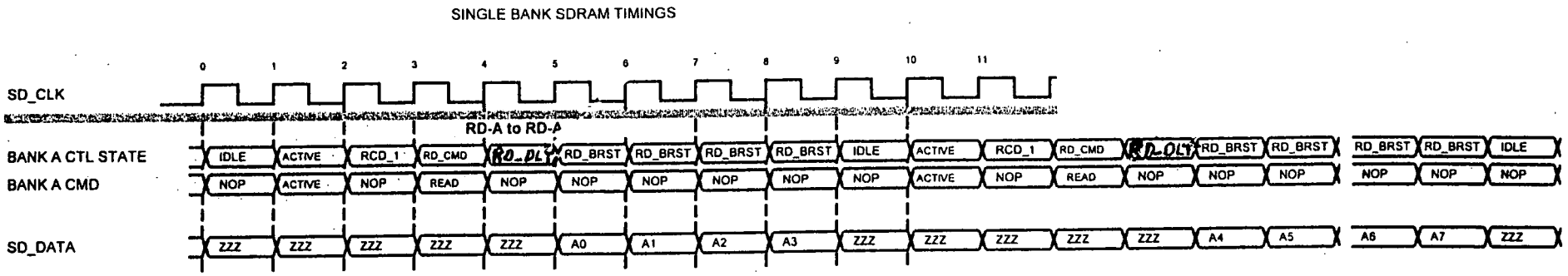
SINGLE BANK SDRAM TIMINGS
0
1
2
3
4
5
6
7
8
9
10
11
SD_CLK
RD-A to RD-A
BANK A CTL STATE
IDLE
ACTIVE
RCD_1
RD_CMD
RD_DLY
RD_BRST
RD_BRST
RD_BRST
RD_BRST
IDLE
ACTIVE
RCD_1
RD_CMD
RD_DLY
RD_BRST
RD_BRST
RD_BRST
RD_BRST
IDLE
BANK A CMD
NOP
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
SD_DATA
ZZZ
ZZZ
ZZZ
ZZZ
ZZZ
A0
A1
A2
A3
ZZZ
ZZZ
ZZZ
ZZZ
ZZZ
A4
A5
A6
A7
ZZZ

FIG. 15A

SINGLE BANK SDRAM TIMINGS

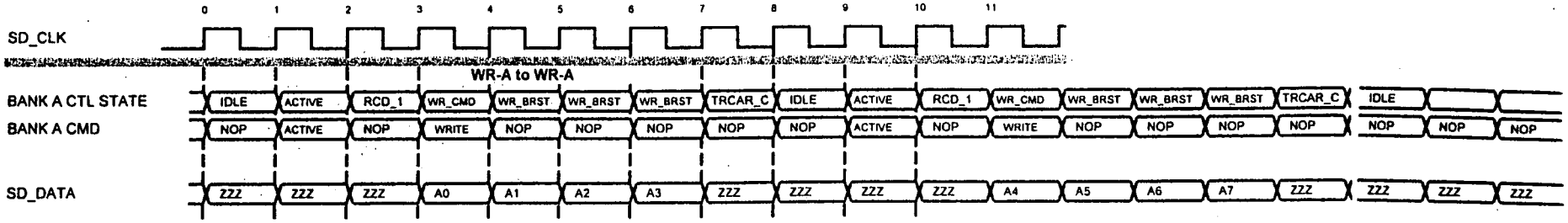

FIG. 15D

TWO BANK SDRAM TIMINGS

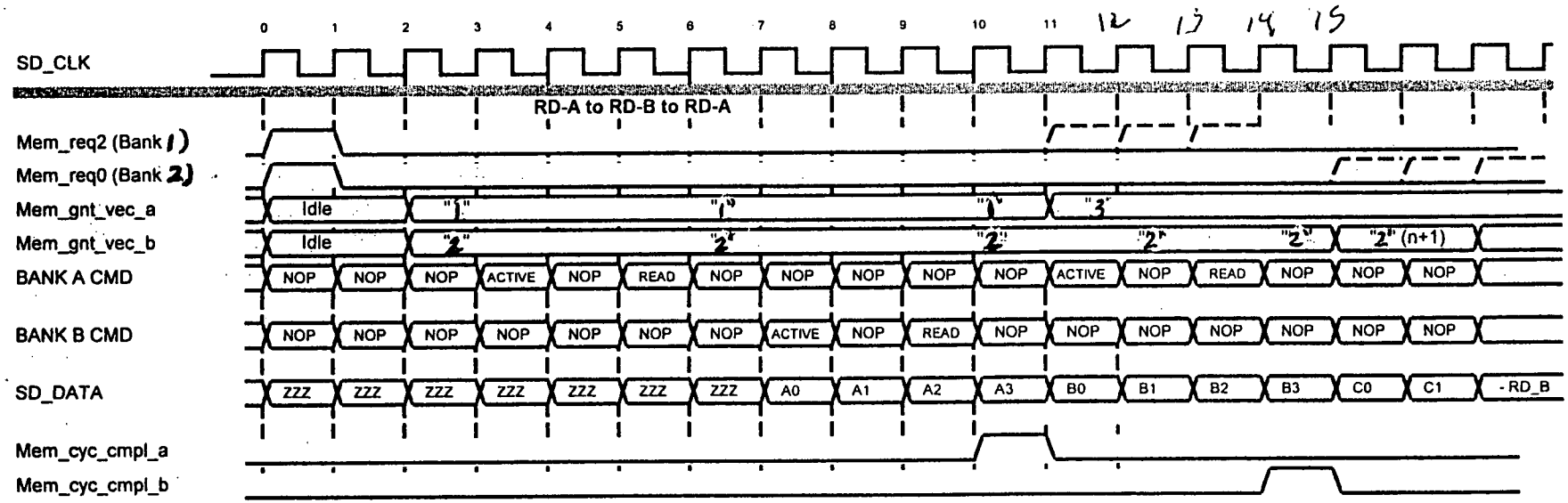

FIG. 6A

TWO BANK SDRAM TIMINGS

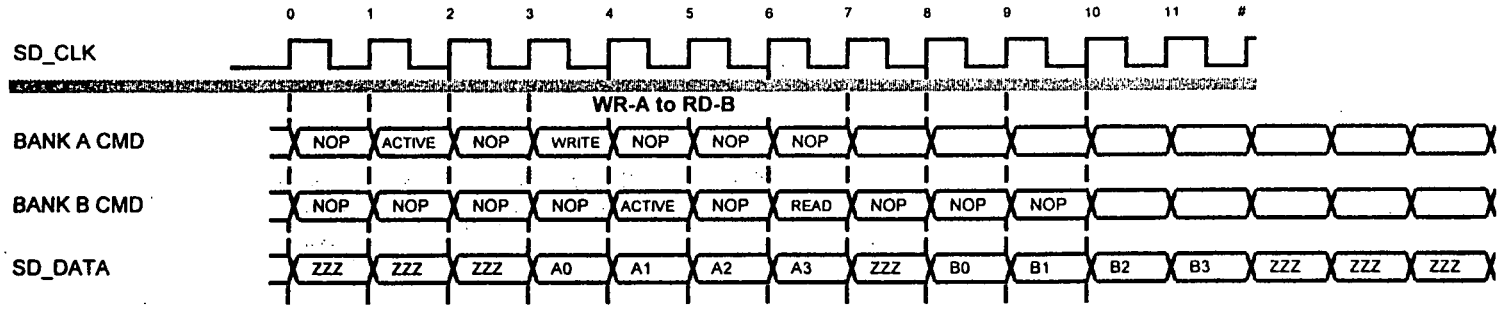

FIG. 16B

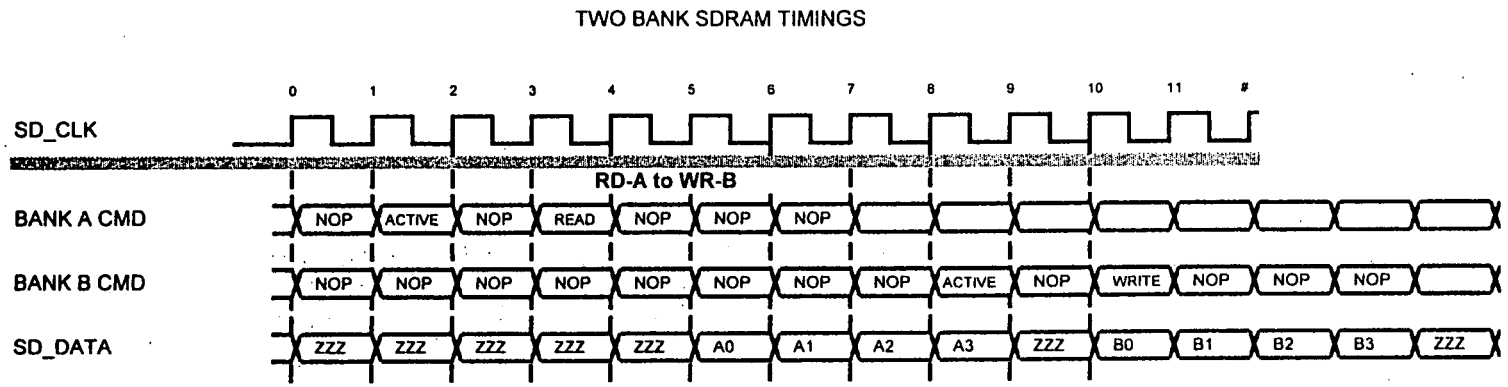
TWO BANK SDRAM TIMINGS
0
1
2
3
4
5
6
7
8
9
10
11
#
SD_CLK
RD-A to WR-B
BANK A CMD
NOP
ACTIVE
NOP
READ
NOP
NOP
NOP
BANK B CMD
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
ACTIVE
NOP
WRITE
NOP
NOP
NOP
SD_DATA
ZZZ
ZZZ
ZZZ
ZZZ
ZZZ
A0
A1
A2
A3
ZZZ
B0
B1
B2
B3
ZZZ

FIG. 16C

TWO BANK SDRAM TIMINGS

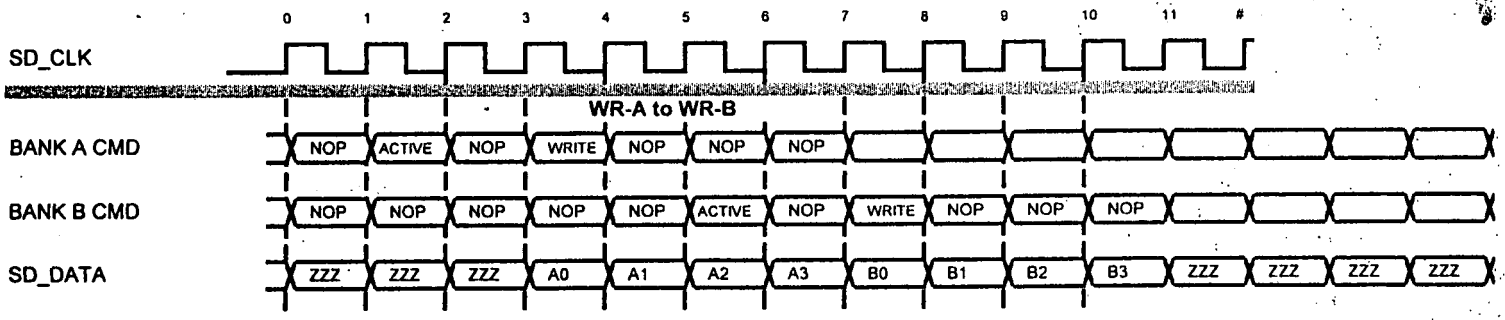

FIG. 16D